

REMARKS

Claims 21-23, 26 and 28 are rejected under 35 U.S.C. 103(a) as obvious over Ryum, *et al.* (U.S. Publication Number 2002/0058388) in view of Arai (U.S. Publication Number 2004/023526) and Emons, *et al.* (U.S. Patent Number 6,100,152). Claims 24 and 25 are rejected under 35 U.S.C. 103(a) as obvious over Ryum, *et al.* in view of Arai, Emons, *et al.* and Kameyama, *et al.* (U.S. Patent No. 5,183,768). Claim 27 is rejected under 35 U.S.C. 103(a) as obvious over Ryum, *et al.* in view of Arai, Emons, *et al.* and Josquin, *et al.* (U.S. Patent No. 5,023,192). Claim 28 is rejected under 35 U.S.C. 103(a) as obvious over Ryum, *et al.* in view of Arai, Emons, *et al.* and Ryum, *et al.* (U.S. Patent No. 5,798,277 - hereinafter Ryum '277). In view of the amendments to the claims and the following remarks, the rejections are respectfully traversed, and reconsideration of the rejections is requested.

In the present invention of claims 21-28, a bipolar transistor includes emitter insulating layers formed on a first base semiconductor layer of a first conductivity type. The emitter insulating layers define an emitter junction portion on the first base semiconductor layer. An emitter region of the second conductivity type is formed on the emitter junction portion on the first base semiconductor layer to contact the first base semiconductor layer through the emitter junction portion. The emitter region has sidewalls being in contact with sidewalls of the emitter insulating layers. Second base semiconductor layer patterns are formed on portions of the first base semiconductor layer except for portions of the first base semiconductor layer having the emitter region and the emitter insulating layers. The second base semiconductor layer patterns are spaced apart from the emitter region by the emitter insulating layers positioned between the emitter region and the second base semiconductor layer patterns.

The claims are amended to clarify that the second base semiconductor layer patterns are spaced apart from the emitter region by the emitter insulating layers positioned between the emitter region and the second base semiconductor layer patterns.

Ryum, *et al.* discloses a base layer (21b and 25) and an emitter layer (21a and 35) that are deposited on a collector layer (see Ryum, *et al.*, Fig. 3a). The emitter layer outside the emitter region is converted to a p++ first base semiconductor electrode film 21a by implanting BF<sub>2</sub> ions, while the emitter layer inside the emitter region 35 remains unchanged and, at the same time, the

base layer outside the emitter region is converted to a p++ second base semiconductor electrode 21b, while the base layer beneath the emitter region 35, i.e. intrinsic base layer 25, remains unchanged (see Ryum, *et al.*, page 3, paragraph 0018). An emitter insulation layer 37 is formed on the emitter layer and the base layer.

Ryum, *et al.* fails to teach or suggest that a bipolar transistor includes second base semiconductor layer patterns that are spaced apart from an emitter region by emitter insulating layers positioned between the emitter region and the second base semiconductor layer patterns, as claimed in claims 21-28. Instead, in Ryum, *et al.*, emitter insulation layer 37 is formed on the first base semiconductor electrode film 21a and the emitter region 35, not between the first base semiconductor electrode film 21a and the emitter region 35. The first base semiconductor electrode film 21a and the emitter region 35 are not spaced apart from one another.

Arai discloses a bipolar transistor with a base semiconductor layer. Arai in no way teaches or suggests second base semiconductor layer patterns. Arai fails to teach or suggest that a bipolar transistor includes second base semiconductor layer patterns that are spaced apart from an emitter region by emitter insulating layers positioned between the emitter region and the second base semiconductor layer patterns, as claimed in claims 21-28.

Emons, *et al.* discloses that an insulating layer 9 is formed on an insulation region 8 in a semiconductor body 10 and a polycrystalline p<sup>+</sup> silicon layer 4 is formed on insulating layer 9. A semiconducting layer 1 is formed on the surface of the semiconductor body 10. Emons, *et al.* in no way teaches or suggests second base semiconductor layer patterns. Emons, *et al.* fails to teach or suggest that a bipolar transistor includes second base semiconductor layer patterns that are spaced apart from an emitter region by emitter insulating layers positioned between the emitter region and the second base semiconductor layer patterns, as claimed in claims 21-28.

Kameyama, *et al.* discloses the use of an SIC region. Kameyama, *et al.* fails to teach or suggest that a bipolar transistor includes second base semiconductor layer patterns that are spaced apart from an emitter region by emitter insulating layers positioned between the emitter region and the second base semiconductor layer patterns, as claimed in claims 21-28.

Josquin, *et al.* discloses the use of a cobalt or titanium silicide layer to improve ohmic contact. Josquin, *et al.* fails to teach or suggest that a bipolar transistor includes second base semiconductor layer patterns that are spaced apart from an emitter region by emitter insulating

layers positioned between the emitter region and the second base semiconductor layer patterns, as claimed in claims 21-28.

Ryum '277 is cited in the Office Action as disclosing that insulating layers are formed of one of oxide layers and nitride layers. Ryum '277 fails to teach or suggest that a bipolar transistor includes second base semiconductor layer patterns that are spaced apart from an emitter region by emitter insulating layers positioned between the emitter region and the second base semiconductor layer patterns, as claimed in claims 21-28.

Hence, none of the Ryum, *et al.* and Arai publications, and Emons, *et al.*, Kameyama, *et al.*, Josquin, *et al.*, and Ryum '277 patents teaches or suggests certain elements of the present invention set forth in claims 21-28. Specifically, none of the references teaches or suggests that a bipolar transistor includes second base semiconductor layer patterns that are spaced apart from an emitter region by emitter insulating layers positioned between the emitter region and the second base semiconductor layer patterns, as claimed in claims 21-28. Accordingly, there is no combination of the references which would provide such teaching or suggestion.

None of the references, taken alone or in combination, teaches or suggests the invention set forth in claims 21-28. Therefore, it is believed that claims 21-28 are allowable over the cited references, and reconsideration of the rejections of claims 21-23, 26 and 28 under 35 U.S.C. § 103(a) based on Ryum, *et al.*, Emons, *et al.* and Arai is respectfully requested. Further, reconsideration of the rejections of claims 24 and 25 under 35 U.S.C. 103(a) based on Ryum, *et al.* in view of Arai, Emons, *et al.* and Kameyama, *et al.* is respectfully requested. In addition, reconsideration of the rejections of claim 27 under 35 U.S.C. 103(a) based on Ryum, *et al.* in view of Arai, Emons, *et al.* and Josquin, *et al.* is respectfully requested. In addition, reconsideration of the rejections of claim 28 under 35 U.S.C. 103(a) based on Ryum, *et al.* in view of Arai, Emons, *et al.* and Ryum '277 is respectfully requested.

Application Number 10/657,867

Amendment dated March 12, 2007

Reply to Office Action of December 12, 2006

In view of the foregoing amendments and remarks, it is believed that all claims pending in the application are in condition for allowance, and such allowance is respectfully solicited. If a telephone conference will expedite prosecution of the application, the Examiner is invited to telephone the undersigned.

Respectfully submitted,

Date: 3/12/07

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